Digital Self Excited Loop Implementation and Experience

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Overview

- Why Self Excited Loop?
- Algorithm Building Blocks
  - Hardware and Sampling
  - Digital Signal Processing Tools
  - Cavity Emulators
- Digital SEL Algorithm Development & Testing
  - Analog SEL
  - Automatic Gain Control
  - Normalizer
  - Phase Pass
  - Discriminator
- Control Algorithm Development & Testing
  - Microphonic Compensator
  - Magnitude and Phase Lock
  - In-Phase and Quadrature Lock
- Field Control Architecture
Why Self Excited Loop?

- Lorentz force detuning
  - Cavity frequency is a function of gradient
  - High Q upgrade cavities
- Generator Driven Resonator
  - Presently used in CEBAF
  - Slowly ramp gradient while mechanical tuners compensate for cavity tune
- Self Excited Loop (SEL)
  - Tolerant of cavity mistuning
  - Quickly bring up cavity gradient without running the tuners
  - Recover faulted cavities in milliseconds instead of minutes

It’s hard to catch a greased pig
Algorithm Independent Hardware

- Down convert 1497MHz to 70MHz
- Sample 70MHz IF with 56Mmps ADC to get In-Phase and Quadrature (I&Q) components
- Apply control algorithm in FPGA
- Produce 70MHz IF with DAC
- Up convert 70MHz to 1497MHz and send to klystron/cavity
Harmonic Sampling

Sample 70 MHz IF at 56 Msps

- Any odd multiple yields I&Q
  - \[ \frac{1}{(2n + 1) / (4 \times 70 \text{MHz})} \]
  - 280, 93.3, 56, 40, … Msps
- Break into 28 Msps I&Q chains
  - I+, -(I-), I+, -(I-), …
  - Q+, -(Q-), Q+, -(Q-), …

Create 70 MHz from 56 Msps I&Q

- Create 14MHz from 56Msps I&Q
  - I, Q, -(I), -(Q), I, Q, -(I), …
  - Also has the effect of mixing 14MHz with 56MHz
- Spectrum includes translation products at 42MHz and 70MHz
- Filter and amplify the 70 MHz component
Field Control Hardware

Digital Board

RF Board
Field Control Hardware

1MHz ADCs & DACs

Field Programmable Gate Array (under PC104)

PC104

Digital Board

Digital I/O

Ref & 56 MHz PLL

1MHz ADCs & DACs

Digital I/O

Ref & 56 MHz PLL

RX Channels

RF Board

DAC

TX
Field Control Hardware
FIR (Finite Impulse Response)

- Stable and linear phase
- Symmetric coefficients allow for “folding”
  - Add two delayed samples together then multiply by common coefficient
  - Half as many multipliers
IIR (Infinite Impulse Response)

- Most like analog filter but can be unstable due to recursion
- Single pole embedded IIR
  - Uses $1-2^{-k}$ as coefficient and $2^{-k}$ for bit growth scaling (bit shifts)
  - Dynamically configurable $k$
  - Cutoff goes as ~ factors of 2

$$H(z) = \frac{N(z)}{D(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_M z^{-M}}{1 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_N z^{-N}}$$

<table>
<thead>
<tr>
<th>$k$</th>
<th>Bandwidth (normalized to 1 Hz)</th>
<th>Rise time (samples)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.1197 MHz</td>
<td>Three</td>
</tr>
<tr>
<td>2</td>
<td>0.0466 MHz</td>
<td>Eight</td>
</tr>
<tr>
<td>3</td>
<td>0.0217 MHz</td>
<td>16</td>
</tr>
<tr>
<td>4</td>
<td>0.0104 MHz</td>
<td>34</td>
</tr>
<tr>
<td>5</td>
<td>0.0051 MHz</td>
<td>69</td>
</tr>
<tr>
<td>6</td>
<td>0.0026 MHz</td>
<td>140</td>
</tr>
<tr>
<td>7</td>
<td>0.0012 MHz</td>
<td>280</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$k$ Value</th>
<th>Bandwidth</th>
<th>$k$ Value</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (none)</td>
<td>4.7 MHz</td>
<td>12</td>
<td>2.2 kHz</td>
</tr>
<tr>
<td>1</td>
<td>3.8 MHz</td>
<td>13</td>
<td>1.1 kHz</td>
</tr>
<tr>
<td>2</td>
<td>2.3 MHz</td>
<td>14</td>
<td>548 Hz</td>
</tr>
<tr>
<td>3</td>
<td>1.2 MHz</td>
<td>15</td>
<td>275 Hz</td>
</tr>
<tr>
<td>4</td>
<td>560 kHz</td>
<td>16</td>
<td>137 Hz</td>
</tr>
<tr>
<td>5</td>
<td>290 kHz</td>
<td>17</td>
<td>69 Hz</td>
</tr>
<tr>
<td>6</td>
<td>140 kHz</td>
<td>18</td>
<td>34 Hz</td>
</tr>
<tr>
<td>7</td>
<td>71 kHz</td>
<td>19</td>
<td>17 Hz</td>
</tr>
<tr>
<td>8</td>
<td>35 kHz</td>
<td>20</td>
<td>9 Hz</td>
</tr>
<tr>
<td>9</td>
<td>18 kHz</td>
<td>21</td>
<td>4 Hz</td>
</tr>
<tr>
<td>10</td>
<td>8.8 kHz</td>
<td>22</td>
<td>2 Hz</td>
</tr>
<tr>
<td>11</td>
<td>4.4 kHz</td>
<td>23</td>
<td>1 Hz</td>
</tr>
</tbody>
</table>
Digital Signal Processing Tools

CIC (Cascaded Integrated Comb)
- Good for decimation
- Sign extend for bit growth, $G = (R \times M)^N$
- Pick a combination that gives a factor of 2
  - $R=4$, $M=2$, $N=3$, $G=512$ (shift 9 bits)
  - $R=8$, $M=1$, $N=2$, $G=64$ (shift 6 bits)

Decimating cascaded integrator-comb (CIC) filter; $N$ stages, $R$ decimation, $M$ delays
Cartesian vs. Polar Coordinates

- Hard to control SEL in I&Q due to spinning phase (frequency detuning)
- Magnitude & Phase preferred
  - More intuitive
  - Simpler equations
Digital Signal Processing Tools

Rotation Matrix

- Cartesian (I&Q) phase shifter
- Look-up-tables for \( \sin(\theta) \) & \( \cos(\theta) \)
- LUT and multipliers can be reused if multiple clock cycles are available (\( \sin(\theta) \) & \( \cos(\theta) \) are 90° apart)

\[
\begin{pmatrix}
    x' \\
y'
\end{pmatrix} = \begin{pmatrix}
    x \\
y
\end{pmatrix} \cdot \begin{bmatrix}
    \cos \theta & -\sin \theta \\
    \sin \theta & \cos \theta
\end{bmatrix}
\]

\[x' = x \cos \theta + y \sin \theta\]
\[y' = y \cos \theta - x \sin \theta\]
**COordinate Rotation Digital Computer**

Add the positive and negative angle rotations to calculate the vector angle. The resultant lies on the X axis with a residual gain of 1.6 due to approximations ($K_i$).

\[
\phi = \sum_i d_i \cdot \arctan(2^{-i})
\]

Add the positive and negative angle rotations to calculate the vector angle.

Divide accumulated X&Y values by $2^{-i}$ (right shift by i) then add or subtract to/from the opposing Y&X depending if the rotated vector was positive or negative for that iteration.

\[
x_{i+1} = K_i \left( y_i - y_i \cdot d_i \cdot 2^{-i} \right)
\]

\[
y_{i+1} = K_i \left( x_i + x_i \cdot d_i \cdot 2^{-i} \right)
\]
Digital Signal Processing Tools

**PID Controller**

\[
c(t) = k_p e(t) + k_i \int_0^t e(\tau) d\tau + k_d \frac{d}{dt} e(t)
\]

\[
c(n) = k_p e[n] + \frac{k_i}{f_s} \sum_{m=0}^{n} e[m] + \frac{f_s}{k_D} (e[n] - e[n-1])
\]

- Classic method works well
- Only P and I have been used but D is available
- Firmware Implementation can be more efficient
Analog Cavity Emulator

Down and up convert to accommodate crystal frequency

Change LO frequency to detune the cavity

1497 MHz

Local Oscillator

$\Sigma$

$\Delta \Phi$

$X^2$

Gradient (eff.)

f = arbitrary! BW < 2 kHz

1497 MHz
Analog Cavity Emulator

- Unity Gain
- BW = 2.86 kHz
- $Q_{eff} = 525,000$
- Non-symmetric due to crystal
Digital Cavity Emulator

- **CIC**: $N$ stages=2, $R$ decimation =4, $M$ delays=1
- **FIR**: 33 taps, $\sim$0.05 normalized cutoff
- **Sample rates** are dynamically adjustable for each stage as well as IIRR ($k=8$: 0.0007 normalized cutoff)
- **Tweak** the sample rate of the last section (37.2 ksp) to give exactly a 45 Hz filter ($Q_{\text{loaded}}=3.3\times10^7$)
Digital Cavity Emulator

**BW** = 45 Hz

**Q_{eff}** = 33,097,000
Digital SEL Algorithm Development

Analog Self Excited Loop

- Noise amplified by klystron then filtered by the cavity
- Limiter amplifies and clips the cavity tone
- Loop phase shifter provides positive feedback to build resonance
- Digitally implement what is in the dashed box
  - Limiter (AGC, Normalizer, or Phase Pass)
  - Loop phase shifter (Rotation Matrix or CORDICs)
Digital SEL Algorithm Development

Automatic Gain Control

- PID Control to stabilize output magnitude
- Tuning the PID control loop was problematic
- Worked as a proof of concept
- Slow lock time
Digital SEL Algorithm Development

Normalizer

- Divide by the magnitude to normalize to 1
- Multiply I&Q by the magnitude set point
- Fixed point division causes errors and noise
- Limited operating range, setup dependent
Digital SEL Algorithm Development

Phase Pass

- 2\textsuperscript{nd} CORDIC converts Mag & Phase to I&Q
- Set Magnitude directly
- Pass frequency info (phase) w/ loop delay
- Fast, stable, intuitive, and simple

Legend

- I, Q
- I
- Q
- Mag
- Phs
Digital SEL Algorithm Development

Phase Pass

2\textsuperscript{nd} CORDIC converts Mag & Phase to I\&Q
Set Magnitude directly
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Legend

- I, Q
- I
- Q
- Mag
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ADC
I\&Q Mux
CIC
FIR
I\&Q Mux
M\&P
To I\&Q
Mux
I\&Q
DeMux
DAC

M_{set}
P_{off}
Digital SEL SRF Cavity Testing

- Measured magnitude, phase, I, and Q sent to diagnostic DACs and plotted on scope
  - When SEL in', phase rolls and magnitude is constant
  - I & Q are sinusoidal with a $90^\circ$ phase shift
- Detuned cavity +/-50 kHz and tracked it with the SEL

- Speed and direction of spin dependent on detuning
- Phase, I, and Q all flatten out if the cavity is tuned to 1497 MHz
- Can excite other pi modes by changing LO frequency

Spinning vector at fixed magnitude
Digital SEL SRF Cavity Testing

- CMTF Tests on Renascence
- Turn-on of detuned cavity
  - Bringing RF up is only limited by cavity fill time
  - No excessive power needed

0 to 21 MV/m in 7 ms!

2 ms/div

~7 ms

External Diode Detector

Internal Gradient Signal

Ptrans Waveform Renascence Cavity 1

Power (W)

-5 0 5 10 15 20 25 30 35

time (ms)
Digital SEL SRF Cavity Testing

- Map cavity using loop phase
- $\pm 45^\circ$ shift corresponds to 3dB points
- Cavity BW $\sim 45\text{Hz}$ ($Q=3.3\times10^7$)
- Easy way to measure cavity $Q$
Digital SEL Firmware

• Pipeline implementation to increase clock rate
• Interleave CORDICs
  – Reuse adds and subtractions, different decisions
  – 56 MHz clock (I&Q to M&P on even clock cycles and M&P to I&Q on odd clock cycles)
Frequency Discriminator Algorithm

- Measure the phase difference over time
  - Configurable via EPICS
    - +/-40Hz to +/-2.5MHz
  - Stepper Motor Channel
    - +/-150 kHz range
  - PZT Channel
    - +/-1.5 kHz range

Frequency is the derivative of phase

\[ F_{err}[n] = P_{mes}[n] - P_{mes}[n-1] \]

Register update rate is adjustable (dt)
**Microphonic Compensator**

- Based on the phase error
  - Rotate the vector to compensate for detune
  - Add magnitude correction

- \( I_{\text{drv}} = Q_{\text{mes}} \times [P_{\text{gain}} \times (P_{\text{set}} - P_{\text{mes}})] \)

- \( Q_{\text{drv}} = -I_{\text{mes}} \times [P_{\text{gain}} \times (P_{\text{set}} - P_{\text{mes}})] \)
Control Algorithm Development

Microphonic Compensation & Magnitude Lock

- Microphonic Compensator locks phase (~.5°)
- PID control of Magnitude needed
- Fought magnitude regulation issues (~.1%)
- Need I&Q clamp, yields up to $2^{1/2}$ magnitude
Control Algorithm Cavity Testing

P\text{mes} & G\text{mes} are flat and drive is compensating for microphonics

\begin{align*}
\text{Measured} & \quad \text{Compensation} \\
\text{Result} & \quad \text{Q} \\
\end{align*}
Control Algorithm Development

Magnitude & Phase Lock

- PID control of Magnitude and Phase
- Phase rollover requires PID to be centered
- Logarithmic magnitude control needed to decouple performance from signal strength
Control Algorithm Development

👍 In-Phase & Quadrature Lock 👍

- PID control of In-Phase & Quadrature
- No phase rollover or logarithmic magnitude control issues
- Stable and meets specs (0.5°, 0.04%)
I&Q Lock Testing

Renascence
$$Q_L = 8.6 \times 10^6$$

Unregulated vs. Regulated microphonics

Open loop
1.1° phase noise

Closed loop
0.068° phase noise

Closed loop
0.0097% amplitude noise
I&Q Lock Testing

Renascence Testing
- Expect 4 Hz rms microphonics for C100 upgrade cavity
  - Worst case six sigma (24 Hz rms) corresponds to 45° detuning for upgrade cavity
  - Piezo induced 45° microphonics on Renascence
- System latency measured as 1.3 us
  - Hardware: 600 ns
  - Firmware: 700 ns

*Image of chart showing phase noise measurement with suppressed 45° detuning and reduced rms phase noise.*
### Tone Mode

- Output 1497 MHz tone at a given magnitude and phase
- Need to add phase spin so the output frequency can be adjusted, 1497 MHz +/- 14 MHz

### Cavity Emulator

- Turn any LLRF module into a cavity for testing
- Loopback or test another module
- $k = 18$, $BW = 34$ Hz ($Q = 4.4 \times 10^7$)
- Need to add Lorentz Force detuning effects
Field Control Architecture

- Cavity Emulator
- I&Q Cavity Lock
- Self Excited Loop
- Tone Generator

- Not shown
  - Discriminator
  - Detune Angle
  - Quench Detect
  - More…
Digital SEL to I&Q Lock Transition

- Spinning phase (sinusoidal I&Q) while in SEL mode
- Forward power spikes and $G_{\text{mes}}$ droops as I&Q lock pulls the arbitrary $I_{\text{mes}}$ & $Q_{\text{mes}}$ to the set points
- Firmware SELs until the spinning phase aligns with desired I&Q set points then switches to I&Q lock
- Eliminates forward power spike and $G_{\text{mes}}$ droop